# M2N1G64TUH8G5F / M2S1G64TUH8G4F / M2N2G64TU8HG5B / M2N2G64TU8HG4B
# 1GB: 128M x 64 / 2GB: 256M x 64
# PC2-5300 / PC2-6400
# Unbuffered DDR2 SO-DIMM

Based on DDR2-667/800 64Mx16 (1GB)/128Mx8 (2GB) SDRAM G-Die

## Features

• Performance:

| Speed Sort | PC2-5300 | PC2-6400 | Unit |
|---|---|---|---|
| | -3C | -AC | |
| DIMM CAS Latency | 5 | 5 | |
| fck – Clock Freqency | 333 | 400 | MHz |
| tck – Clock Cycle | 3 | 2.5 | ns |
| Data Transfer Speed | 667 | 800 | Mbps |

• 200-Pin Small Outline Dual In-Line Memory Module (SO-DIMM)
• 1GB: 128Mx64 Unbuffered DDR2 SO-DIMM based on 64M x16 DDR2 SDRAM G-Die devices.
• 2GB: 256Mx64 Unbuffered DDR2 SO-DIMM based on 128M x8 DDR2 SDRAM G-Die devices.
• Intended for 333MHz and 400MHz applications
• Inputs and outputs are SSTL-18 compatible
• $V_{DD} = V_{DDQ} = 1.8V \pm 0.1V$
• SDRAMs have 8 internal banks for concurrent operation
• Differential clock inputs
• Data is read or written on both clock edges
• DRAM DLL aligns DQ and DQS transitions with clock transitions.
• Address and control signals are fully synchronous to positive clock edge
• Auto Refresh (CBR) and Self Refresh Modes
• Automatic and controlled precharge commands
• Programmable Operation:
  - DIMM $\overline{CAS}$ Latency: 3, 4, 5
  - Burst Type: Sequential or Interleave
  - Burst Length: 4, 8
  - Operation: Burst Read and Write
• 13/10/2 Addressing (1GB)
• 14/10/2 Addressing (2GB)
• 7.8 μs Max. Average Periodic Refresh Interval
• Serial Presence Detect
• Gold contacts
• 1GB module's SDRAMs are 84-ball BGA Package
• 2GB module's SDRAMs are 60-ball BGA Package
• RoHS compliance

## Description

M2N1G64TUH8G5F / M2S1G64TUH8G4F / M2N2G64TU8HG5B / M2N2G64TU8HG4B are unbuffered 200-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Small Outline Dual In-Line Memory Module (SO-DIMM), organized as two ranks of 128Mx64 (1GB)/256Mx64 (2GB) high-speed memory array. M2N1G64TUH8G5F / M2S1G64TUH8G4F uses eight 64Mx16 84-ball BGA packaged devices and M2N2G64TU8HG5B / M2N2G64TU8HG4B uses sixteen 128Mx8 60-ball BGA packaged devices. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All Elixir DDR2 SODIMMs provide a high-performance, flexible 8-byte interface in a space-saving footprint.

The DIMM is intended for use in applications operating of 333MHz/400MHz clock speeds and achieves high-speed data transfer speed of 667Mbps/800Mbps. Prior to any access operation, the device $\overline{CAS}$ latency and burst/length/operation type must be programmed into the DIMM by address inputs A0-A12 (1GB) / A0-A13 (2GB) and I/O inputs BA0, BA1 and BA2 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial EEPROM using a standard IIC protocol. The first 128 bytes of SPD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.


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## Ordering Information

| Part Number | Speed | | | Organization | Power | Leads | Note |
|---|---|---|---|---|---|---|---|
| M2N2G64TU8HG5B-AC | DDR2-800 | PC2-6400 | 400MHz (2.5ns @ CL = 5) | 256Mx64 | 1.8V | Gold | |
| M2N2G64TU8HG5B-3C | DDR2-667 | PC2-5300 | 333MHz (3.0ns @ CL = 5) | | | | |
| M2N2G64TU8HG4B-AC | DDR2-800 | PC2-6400 | 400MHz (2.5ns @ CL = 5) | | | | |
| M2N1G64TUH8G5F-AC | DDR2-800 | PC2-6400 | 400MHz (2.5ns @ CL = 5) | 128Mx64 | | | |
| M2N1G64TUH8G5F-3C | DDR2-667 | PC2-5300 | 333MHz (3.0ns @ CL = 5) | | | | |
| M2S1G64TUH8G4F-AC | DDR2-800 | PC2-6400 | 400MHz (2.5ns @ CL = 5) | | | | |

## Pin Description

| | | | |
|---|---|---|---|
| CK0, CK1, $\overline{CK0}$, $\overline{CK1}$ | Differential Clock Inputs | DQ0-DQ63 | Data input/output |
| CKE0, CKE1 | Clock Enable | DQS0-DQS7 | Bidirectional data strobes |
| $\overline{RAS}$ | Row Address Strobe | $\overline{DQS0}$-$\overline{DQS7}$ | Differential data strobes |
| $\overline{CAS}$ | Column Address Strobe | DM0-DM7 | Input Data Masks |
| $\overline{WE}$ | Write Enable | $V_{DD}$ | Power (1.8V) |
| $\overline{CS0}$, $\overline{CS1}$ | Chip Selects | $V_{REF}$ | Ref. Voltage for SSTL_18 inputs |
| A0-A9 A11-A13 | Row Address Inputs | $V_{DDSPD}$ | Serial EEPROM positive power supply |
| A0-A9 | Column Address Inputs | $V_{SS}$ | Ground |
| A10/AP | Column Address Input/Auto-precharge | SCL | Serial Presence Detect Clock Input |
| BA0, BA1, BA2 | SDRAM Bank Address Inputs | SDA | Serial Presence Detect Data input/output |
| ODT0, ODT1 | Active termination control lines | SA0, SA1 | Serial Presence Detect Address Inputs |
| NC | No Connect | | |

Note: A13 is for 2GB modules only.


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## Pinout

| Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{REF}$ | 2 | $V_{SS}$ | 51 | DQS2 | 52 | DM2 | 101 | A1 | 102 | A0 | 151 | DQ42 | 152 | DQ46 |
| 3 | $V_{SS}$ | 4 | DQ4 | 53 | $V_{SS}$ | 54 | $V_{SS}$ | 103 | $V_{DD}$ | 104 | $V_{DD}$ | 153 | DQ43 | 154 | DQ47 |
| 5 | DQ0 | 6 | DQ5 | 55 | DQ18 | 56 | DQ22 | 105 | A10/AP | 106 | BA1 | 155 | $V_{SS}$ | 156 | $V_{SS}$ |
| 7 | DQ1 | 8 | $V_{SS}$ | 57 | DQ19 | 58 | DQ23 | 107 | BA0 | 108 | $\overline{RAS}$ | 157 | DQ48 | 158 | DQ52 |
| 9 | $V_{SS}$ | 10 | DM0 | 59 | $V_{SS}$ | 60 | $V_{SS}$ | 109 | $\overline{WE}$ | 110 | $\overline{CS0}$ | 159 | DQ49 | 160 | DQ53 |
| 11 | $\overline{DQS0}$ | 12 | $V_{SS}$ | 61 | DQ24 | 62 | DQ28 | 111 | $V_{DD}$ | 112 | $V_{DD}$ | 161 | $V_{SS}$ | 162 | $V_{SS}$ |
| 13 | DQS0 | 14 | DQ6 | 63 | DQ25 | 64 | DQ29 | 113 | $\overline{CAS}$ | 114 | ODT0 | 163 | NC | 164 | CK1 |
| 15 | $V_{SS}$ | 16 | DQ7 | 65 | $V_{SS}$ | 66 | $V_{SS}$ | 115 | $\overline{CS1}$ | 116 | A13/NC | 165 | $V_{SS}$ | 166 | $\overline{CK1}$ |
| 17 | DQ2 | 18 | $V_{SS}$ | 67 | DM3 | 68 | $\overline{DQS3}$ | 117 | $V_{DD}$ | 118 | $V_{DD}$ | 167 | $\overline{DQS6}$ | 168 | $V_{SS}$ |
| 19 | DQ3 | 20 | DQ12 | 69 | NC | 70 | DQS3 | 119 | ODT1 | 120 | NC | 169 | DQS6 | 170 | DM6 |
| 21 | $V_{SS}$ | 22 | DQ13 | 71 | $V_{SS}$ | 72 | $V_{SS}$ | 121 | $V_{SS}$ | 122 | $V_{SS}$ | 171 | $V_{SS}$ | 172 | $V_{SS}$ |
| 23 | DQ8 | 24 | $V_{SS}$ | 73 | DQ26 | 74 | DQ30 | 123 | DQ32 | 124 | DQ36 | 173 | DQ50 | 174 | DQ54 |
| 25 | DQ9 | 26 | DM1 | 75 | DQ27 | 76 | DQ31 | 125 | DQ33 | 126 | DQ37 | 175 | DQ51 | 176 | DQ55 |
| 27 | $V_{SS}$ | 28 | $V_{SS}$ | 77 | $V_{SS}$ | 78 | $V_{SS}$ | 127 | $V_{SS}$ | 128 | $V_{SS}$ | 177 | $V_{SS}$ | 178 | $V_{SS}$ |
| 29 | $\overline{DQS1}$ | 30 | CK0 | 79 | CKE0 | 80 | CKE1 | 129 | $\overline{DQS4}$ | 130 | DM4 | 179 | DQ56 | 180 | DQ60 |
| 31 | DQS1 | 32 | $\overline{CK0}$ | 81 | $V_{DD}$ | 82 | $V_{DD}$ | 131 | DQS4 | 132 | $V_{SS}$ | 181 | DQ57 | 182 | DQ61 |
| 33 | $V_{SS}$ | 34 | $V_{SS}$ | 83 | NC | 84 | NC | 133 | $V_{SS}$ | 134 | DQ38 | 183 | $V_{SS}$ | 184 | $V_{SS}$ |
| 35 | DQ10 | 36 | DQ14 | 85 | BA2 | 86 | NC | 135 | DQ34 | 136 | DQ39 | 185 | DM7 | 186 | $\overline{DQS7}$ |
| 37 | DQ11 | 38 | DQ15 | 87 | $V_{DD}$ | 88 | $V_{DD}$ | 137 | DQ35 | 138 | $V_{SS}$ | 187 | $V_{SS}$ | 188 | DQS7 |
| 39 | $V_{SS}$ | 40 | $V_{SS}$ | 89 | A12 | 90 | A11 | 139 | $V_{SS}$ | 140 | DQ44 | 189 | DQ58 | 190 | $V_{SS}$ |
| 41 | $V_{SS}$ | 42 | $V_{SS}$ | 91 | A9 | 92 | A7 | 141 | DQ40 | 142 | DQ45 | 191 | DQ59 | 192 | DQ62 |
| 43 | DQ16 | 44 | DQ20 | 93 | A8 | 94 | A6 | 143 | DQ41 | 144 | $V_{SS}$ | 193 | $V_{SS}$ | 194 | DQ63 |
| 45 | DQ17 | 46 | DQ21 | 95 | $V_{DD}$ | 96 | $V_{DD}$ | 145 | $V_{SS}$ | 146 | $\overline{DQS5}$ | 195 | SDA | 196 | $V_{SS}$ |
| 47 | $V_{SS}$ | 48 | $V_{SS}$ | 97 | A5 | 98 | A4 | 147 | DM5 | 148 | DQS5 | 197 | SCL | 198 | SA0 |
| 49 | $\overline{DQS2}$ | 50 | NC | 99 | A3 | 100 | A2 | 149 | $V_{SS}$ | 150 | $V_{SS}$ | 199 | $V_{DDSPD}$ | 200 | SA1 |

Note: All pin assignments are consistent for all 8-byte unbuffered versions.
A13 is for 2GB modules only.


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## Input/Output Functional Description

| Symbol | Type | Polarity | Function |
|---|---|---|---|
| CK0, CK1 | (SSTL) | Positive Edge | The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks. |
| $\overline{CK0}$, $\overline{CK1}$ | (SSTL) | Negative Edge | The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. |
| CKE0, CKE1 | (SSTL) | Active High | Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode. |
| $\overline{CS0}$, $\overline{CS1}$ | (SSTL) | Active Low | Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | (SSTL) | Active Low | When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM. |
| $V_{REF}$ | Supply | | Reference voltage for SSTL-18 inputs |
| ODT0, ODT1 | Input | Active High | On-Die Termination control signals |
| BA0, BA1, BA2 | (SSTL) | - | Selects which SDRAM bank is to be active. |
| A0 – A9<br>A10/AP<br>A11, A12/A13 | (SSTL) | - | During a Bank Activate command cycle, A0-A12/A13 define the row address (RA0-RA12/RA13) when sampled at the rising clock edge. A13 applies on 2GB SODIMM only.<br>During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1/BA2 define the bank to be precharged. If AP is low, autoprecharge is disabled.<br>During a Precharge command cycle, AP is used in conjunction with BA0/BA1/BA2 to control which bank(s) to precharge. If AP is high all 8 banks will be precharged regardless of the state of BA0/BA1/BA2. If AP is low, then BA0/BA1/BA2 are used to define which bank to pre-charge. |
| DQ0 – DQ63 | (SSTL) | Active High | Data and Check Bit Input/Output pins. |
| $V_{DD}$, $V_{SS}$ | Supply | | Power and ground for the DDR2 SDRAM input buffers and core logic |
| DQS0 – DQS7<br>$\overline{DQS0}$ – $\overline{DQS7}$ | (SSTL) | Negative and Positive Edge | Data strobe for input and output data |
| DM0 – DM7 | Input | Active High | The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules. |
| SA0 – SA1 | | - | Address inputs. Connected to either VDD or VSS on the system board to configure the Serial Presence Detect EEPROM address. |
| SDA | | - | This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V DD to act as a pull-up. |
| SCL | | - | This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V DD to act as a pull-up. |
| $V_{DDSPD}$ | Supply | | Serial EEPROM positive power supply. |


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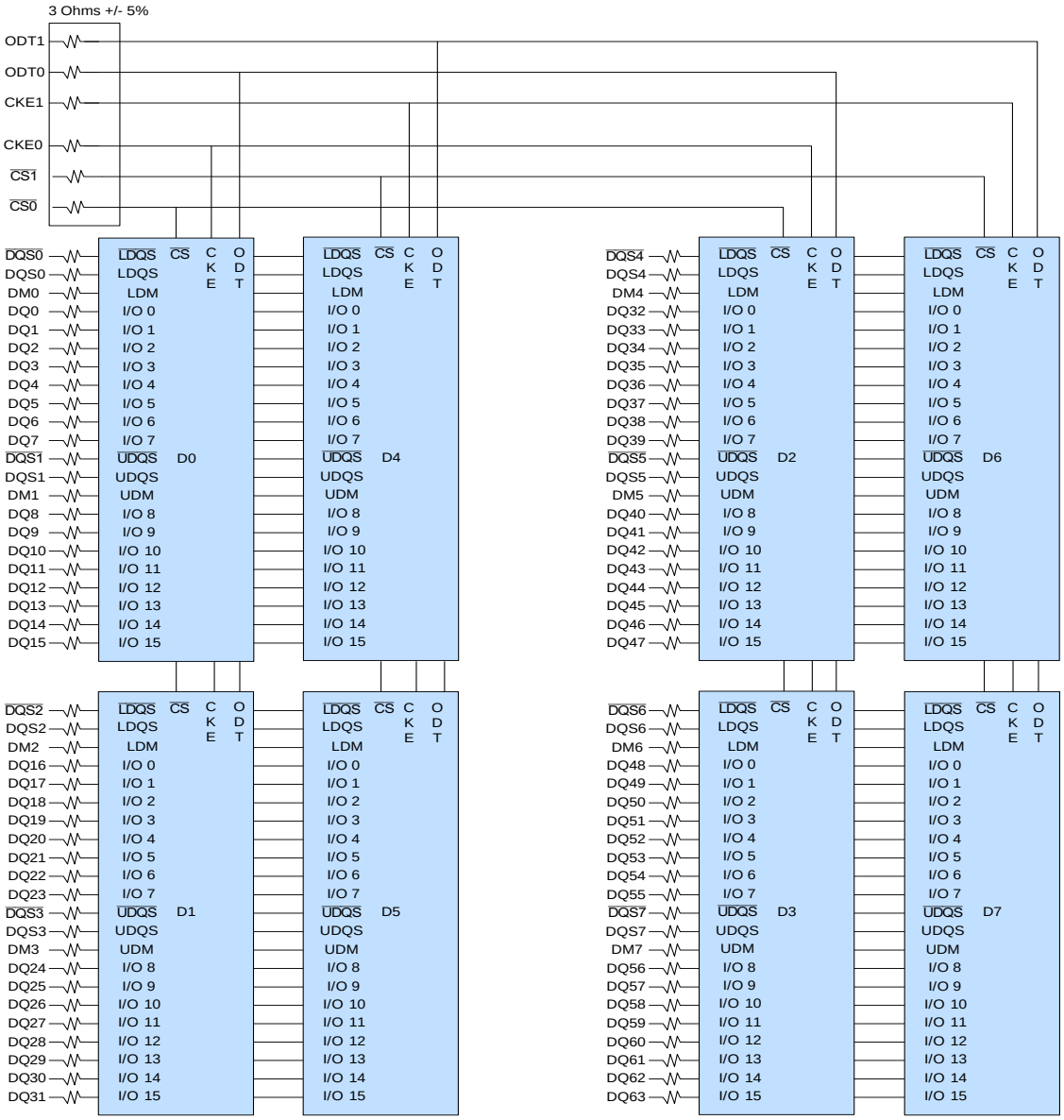
## Functional Block Diagram

[1GB – 2 Ranks, 64Mx16 DDR2 SDRAMs]




**Notes**

1. DQ wiring may differ from that described in this drawing.
2. DQ/DQS/DM/CKE/S S relationships are maintained as shown.
3. DQ/DQS/DM/DQS resistors are 22 +/- 5% Ohms
4. $V_{DDID}$ strap connections (for memory device $V_{DD}$, $V_{DDQ}$):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN ($V_{SS}$): $V_{DD}$ is not equal to $V_{DDQ}$



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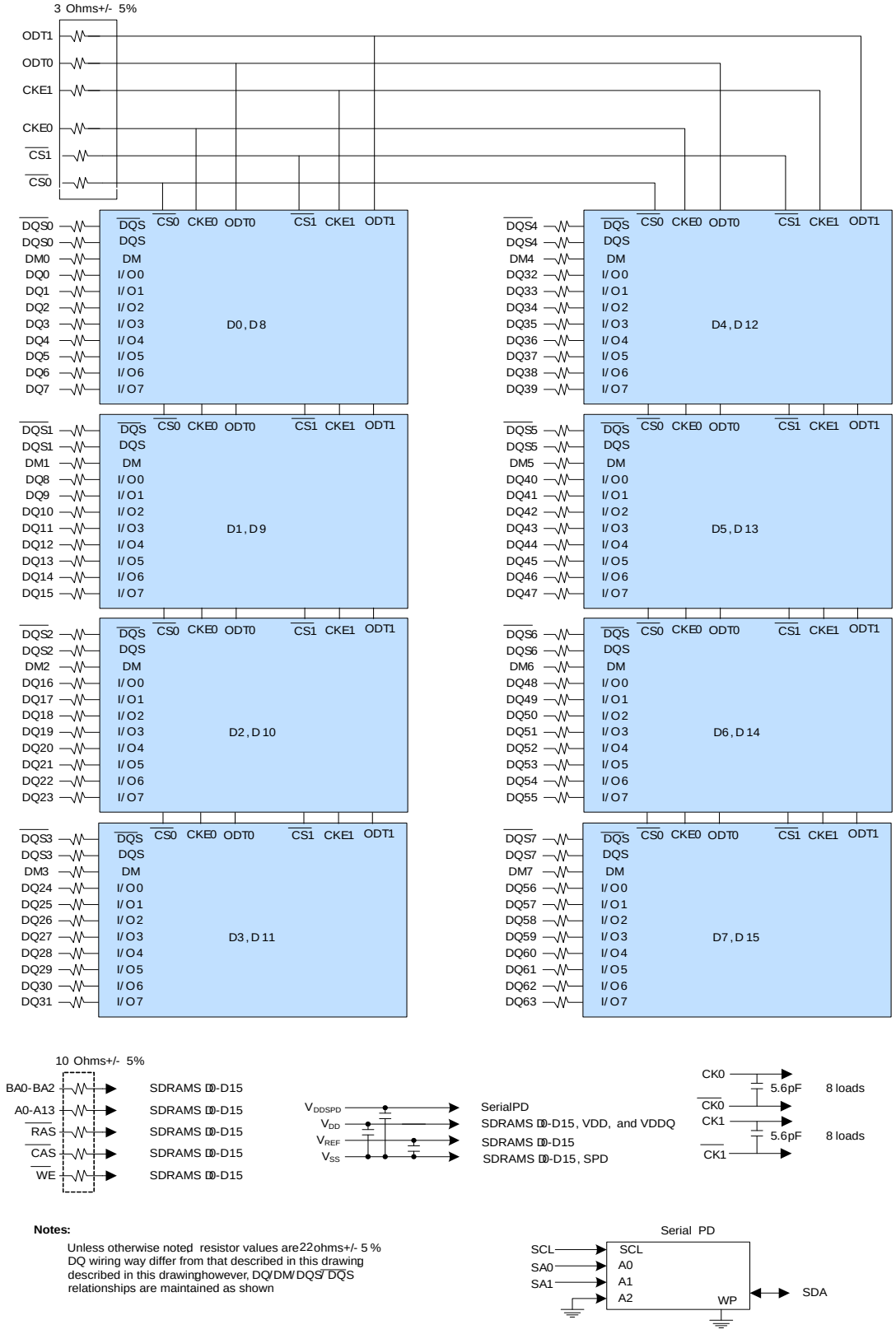
## Functional Block Diagram

[2GB – 2 Ranks, 128M x8 DDR2 SDRAMs]




**Notes:**

Unless otherwise noted resistor values are 22 ohms +/- 5 %
DQ wiring may differ from that described in this drawing however, DQ/DM/DQS/DQS relationships are maintained as shown



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## Serial Presence Detect (1GB – 2 Ranks, 64Mx16 DDR2 SDRAMs) (Part 1 of 2)

| Byte | Description | Serial PD Data Entry (Hex.) | | Note |
|---|---|---|---|---|
| | | -3C | -AC | |
| 0 | Number of Serial PD Bytes Written during Production | 80 | 80 | |
| 1 | Total Number of Bytes in Serial PD device | 08 | 08 | |
| 2 | Fundamental Memory Type | 08 | 08 | |
| 3 | Number of Row Addresses on Assembly | 0D | 0D | |
| 4 | Number of Column Addresses on Assembly | 0A | 0A | |
| 5 | Number of DIMM Ranks, Package, and Height | 61 | 61 | |
| 6 | Data Width of Assembly | 40 | 40 | |
| 7 | Reserved | 00 | 00 | |
| 8 | Voltage Interface Level of this Assembly | 05 | 05 | |
| 9 | DDR2 SDRAM Device Cycle Time at CL=5 | 30 | 25 | |
| 10 | DDR2 SDRAM Device Access Time ($t_{ac}$) from Clock at CL=5 | 45 | 40 | |
| 11 | DIMM Configuration Type | 00 | 00 | |
| 12 | Refresh Rate/Type | 82 | 82 | |
| 13 | Primary DDR2 SDRAM Width | 10 | 10 | |
| 14 | Error Checking DDR2 SDRAM Device Width | 00 | 00 | |
| 15 | Reserved | 00 | 00 | |
| 16 | DDR2 SDRAM Device Attributes: Burst Length Supported | 0C | 0C | |
| 17 | DDR2 SDRAM Device Attributes: Number of Device Banks | 08 | 08 | |
| 18 | DDR2 SDRAM Device Attributes: $\overline{CAS}$ Latencies Supported | 38 | 38 | |
| 19 | DIMM Mechanical Characteristics | 01 | 01 | |
| 20 | DDR2 SDRAM DIMM Type Information | 04 | 04 | |
| 21 | DDR2 SDRAM Module Attributes | 00 | 00 | |
| 22 | DDR2 SDRAM Device Attributes: General | 03 | 03 | |
| 23 | Minimum Clock Cycle at CL=4 | 3D | 3D | |
| 24 | Maximum Data Access Time from Clock at CL=4 | 50 | 50 | |
| 25 | Minimum Clock Cycle Time at CL=3 | 50 | 50 | |
| 26 | Maximum Data Access Time from Clock at CL=3 | 60 | 60 | |
| 27 | Minimum Row Precharge Time ($t_{RP}$) | 3C | 32 | |
| 28 | Minimum Row Active to Row Active delay ($t_{RRD}$) | 28 | 28 | |
| 29 | Minimum $\overline{RAS}$ to $\overline{CAS}$ delay ($t_{RCD}$) | 3C | 32 | |
| 30 | Minimum Active to Precharge Time ($t_{RAS}$) | 2D | 2D | |
| 31 | Module Rank Density | 80 | 80 | |
| 32 | Address and Command Setup Time Before Clock ($t_{IS}$) | 20 | 17 | |
| 33 | Address and Command Hold Time After Clock ($t_{IH}$) | 27 | 25 | |
| 34 | Data Input Setup Time Before Clock ($t_{DS}$) | 10 | 05 | |
| 35 | Data Input Hold Time After Clock (tDH) | 17 | 12 | |
| 36 | Write Recovery Time ($t_{WR}$) | 3C | 3C | |


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## Serial Presence Detect (1GB – 2 Ranks, 64Mx16 DDR2 SDRAMs) (Part 2 of 2)

| Byte | Description | Serial PD Data Entry (Hex.) | | Note |
|---|---|---|---|---|
| | | -3C | -AC | |
| 37 | Internal Write to Read Command delay ($t_{WTR}$) | 1E | 1E | |
| 38 | Internal Read to Precharge delay ($t_{RTP}$) | 1E | 1E | |
| 39 | Reserved | 00 | 00 | |
| 40 | Extension of Byte 41 $t_{RC}$ and Byte 42 $t_{RFC}$ | 06 | 36 | |
| 41 | Minimum Core Cycle Time ($t_{RC}$) | 3C | 39 | |
| 42 | Min. Auto Refresh Command Cycle Time ($t_{RFC}$) | 7F | 7F | |
| 43 | Maximum Clock Cycle Time ($t_{CK}$) | 80 | 80 | |
| 44 | Max. DQS-DQ Skew Factor (tQHS) | 18 | 14 | |
| 45 | Read Data Hold Skew Factor (tQHS) | 22 | 1E | |
| 46-61 | Reserved | -- | -- | |
| 62 | SPD Reversion | 13 | 13 | |
| 63 | Checksum for Byte 0-62 | A6 | 8C | |
| 64-71 | Manufacturer's JEDEC ID Code | -- | -- | |
| 72 | Module Manufacturing Location | 00 | 00 | |
| 73-91 | Module Part number | -- | -- | |
| 92-255 | Reserved | -- | -- | |


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## Serial Presence Detect (2GB – 2 Ranks, 128Mx8 DDR2 SDRAMs) (Part 1 of 2)

| Byte | Description | Serial PD Data Entry (Hex.) | | Note |
|---|---|---|---|---|
| | | -3C | -AC | |
| 0 | Number of Serial PD Bytes Written during Production | 80 | 80 | |
| 1 | Total Number of Bytes in Serial PD device | 08 | 08 | |
| 2 | Fundamental Memory Type | 08 | 08 | |
| 3 | Number of Row Addresses on Assembly | 0E | 0E | |
| 4 | Number of Column Addresses on Assembly | 0A | 0A | |
| 5 | Number of DIMM Ranks, Package, and Height | 61 | 61 | |
| 6 | Data Width of Assembly | 40 | 40 | |
| 7 | Reserved | 00 | 00 | |
| 8 | Voltage Interface Level of this Assembly | 05 | 05 | |
| 9 | DDR2 SDRAM Device Cycle Time at CL=5 | 30 | 25 | |
| 10 | DDR2 SDRAM Device Access Time ($t_{ac}$) from Clock at CL=5 | 45 | 40 | |
| 11 | DIMM Configuration Type | 00 | 00 | |
| 12 | Refresh Rate/Type | 82 | 82 | |
| 13 | Primary DDR2 SDRAM Width | 08 | 08 | |
| 14 | Error Checking DDR2 SDRAM Device Width | 00 | 00 | |
| 15 | Reserved | 00 | 00 | |
| 16 | DDR2 SDRAM Device Attributes: Burst Length Supported | 0C | 0C | |
| 17 | DDR2 SDRAM Device Attributes: Number of Device Banks | 08 | 08 | |
| 18 | DDR2 SDRAM Device Attributes: $\overline{CAS}$ Latencies Supported | 38 | 38 | |
| 19 | DIMM Mechanical Characteristics | 01 | 01 | |
| 20 | DDR2 SDRAM DIMM Type Information | 04 | 04 | |
| 21 | DDR2 SDRAM Module Attributes | 00 | 00 | |
| 22 | DDR2 SDRAM Device Attributes: General | 03 | 03 | |
| 23 | Minimum Clock Cycle at CL=4 | 3D | 3D | |
| 24 | Maximum Data Access Time from Clock at CL=4 | 50 | 50 | |
| 25 | Minimum Clock Cycle Time at CL=3 | 50 | 50 | |
| 26 | Maximum Data Access Time from Clock at CL=3 | 60 | 60 | |
| 27 | Minimum Row Precharge Time ($t_{RP}$) | 3C | 32 | |
| 28 | Minimum Row Active to Row Active delay ($t_{RRD}$) | 1E | 1E | |
| 29 | Minimum $\overline{RAS}$ to $\overline{CAS}$ delay ($t_{RCD}$) | 3C | 32 | |
| 30 | Minimum Active to Precharge Time ($t_{RAS}$) | 2D | 2D | |
| 31 | Module Rank Density | 01 | 01 | |
| 32 | Address and Command Setup Time Before Clock ($t_{IS}$) | 20 | 17 | |
| 33 | Address and Command Hold Time After Clock ($t_{IH}$) | 27 | 25 | |
| 34 | Data Input Setup Time Before Clock ($t_{DS}$) | 10 | 05 | |
| 35 | Data Input Hold Time After Clock (tDH) | 17 | 12 | |
| 36 | Write Recovery Time ($t_{WR}$) | 3C | 3C | |


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## Serial Presence Detect (2GB – 2 Ranks, 128 M x 8 DDR2 SDRAMs) (Part 2 of 2)

| Byte | Description | Serial PD Data Entry (Hex.) | | Note |
|---|---|---|---|---|
| | | -3C | -AC | |
| 37 | Internal Write to Read Command delay ($t_{WTR}$) | 1E | 1E | |
| 38 | Internal Read to Precharge delay ($t_{RTP}$) | 1E | 1E | |
| 39 | Reserved | 00 | 00 | |
| 40 | Extension of Byte 41 $t_{RC}$ and Byte 42 $t_{RFC}$ | 06 | 36 | |
| 41 | Minimum Core Cycle Time ($t_{RC}$) | 3C | 39 | |
| 42 | Min. Auto Refresh Command Cycle Time ($t_{RFC}$) | 7F | 7F | |
| 43 | Maximum Clock Cycle Time ($t_{CK}$) | 80 | 80 | |
| 44 | Max. DQS-DQ Skew Factor (tQHS) | 18 | 14 | |
| 45 | Read Data Hold Skew Factor (tQHS) | 22 | 1E | |
| 46-61 | Reserved | -- | -- | |
| 62 | SPD Reversion | 13 | 13 | |
| 63 | Checksum for Byte 0-62 | 16 | FC | |
| 64-71 | Manufacturer's JEDEC ID Code | -- | -- | |
| 72 | Module Manufacturing Location | 00 | 00 | |
| 73-91 | Module Part number | -- | -- | |
| 92-255 | Reserved | -- | -- | |


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## Environmental Requirements

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $T_{OPR}$ | Operating Temperature (ambient) | 0 to 65 | °C |
| $H_{OPR}$ | Operating Humidity (relative) | 10 to 90 | % |
| $T_{STG}$ | Storage Temperature | -50 to 100 | °C |
| $H_{STG}$ | Storage Humidity (without condensation) | 5 to 95 | % |
| | Barometric pressure (operating & storage) up to 9850ft. | 105 to 69 | kPa |

**Note**: Stress greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

## Absolute Maximum DC Ratings

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $V_{DD}$ | Voltage on VDD pins relative to Vss | -1.0 to +2.3 | V |
| $V_{DDQ}$ | Voltage on VDDQ pins relative to Vss | -0.5 to +2.3 | V |
| $V_{DDL}$ | Voltage on VDDL pins relative to Vss | -0.5 to +2.3 | V |
| $V_{IN}$, $V_{OUT}$ | Voltage on I/O pins relative to Vss | -0.5 to +2.3 | V |
| $T_{STG}$ | Storage Temperature (Plastic) | -55 to +100 | °C |

**Note**: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
Storage temperature is the case surface temperature on the center/top side of the DRAM.

## Operating temperature Conditions

| Symbol | Parameter | Rating | Units | Note |
|---|---|---|---|---|
| $T_{CASE}$ | Operating Temperature (Ambient) | 0 to 95 | °C | 1 |

**Note:**
1. Case temperature is measured at top and center side of any DRAMs.
2. $t_{CASE}$ > 85°C ➔ $t_{REFI}$ = 3.9 µs

## DC Electrical Characteristics and Operating Conditions

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 1.7 | 1.9 | V | 1 |
| $V_{DDL}$ | DLL Supply Voltage | 1.7 | 1.9 | V | 1 |
| $V_{DDQ}$ | Output Supply Voltage | 1.7 | 1.9 | V | 1 |
| $V_{SS}$, $V_{SSQ}$ | Supply Voltage, I/O Supply Voltage | 0 | 0 | V | |
| $V_{REF}$ | Input Reference Voltage | 0.49$V_{DDQ}$ | 0.51$V_{DDQ}$ | V | 1, 2 |
| $V_{TT}$ | Termination Voltage | $V_{REF}$ – 0.04 | $V_{REF}$ + 0.04 | V | 3 |

**Note:**
1. There is no specific device VDD supply voltage requirement for SSTL_18 compliance. However, VDDQ must be less than or equal to VDD under all conditions.
2. $V_{REF}$ is expected to be equal to 0.5 $V_{DDQ}$ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on $V_{REF}$ may not exceed 2% of the DC value.
3. VTT of transmitting device must track VREF of receiving device.


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## ODT DC Electrical Characteristics

| Parameter/Condition | Symbol | Min. | Nom. | Max. | Units | Note |
|---|---|---|---|---|---|---|
| Rtt effective impedance value for EMRS(A6,A2)=0,1; 75ohm | Rtt1(eff) | 60 | 75 | 90 | ohm | 1 |
| Rtt effective impedance value for EMRS(A6,A2)=1,0; 150ohm | Rtt2(eff) | 120 | 150 | 180 | ohm | 1 |
| Rtt effective impedance value for EMRS(A6,A2)=1,1; 50ohm | Rtt3(eff) | 40 | 50 | 60 | ohm | 1 |
| Deviation of $V_M$ with respect to VDDQ/2 | Delta VM | -6 | | +6 | % | 1 |
| Note1: Test condition for Rtt measurements. | | | | | | |

`

## Input AC/DC logic level

| Symbol | Parameter | PC2-5300 | | PC2-6400 | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $V_{IH\ (AC)}$ | Input High (Logic1) Voltage | $V_{REF}$ + 0.200 | - | $V_{REF}$ + 0.200 | - | V |
| $V_{IL\ (AC)}$ | Input Low (Logic0) Voltage | - | $V_{REF}$ – 0.200 | - | $V_{REF}$ – 0.200 | V |
| $V_{IH\ (DC)}$ | Input High (Logic1) Voltage | $V_{REF}$ + 0.125 | $V_{DDQ}$ + 0.3 | $V_{REF}$ + 0.125 | $V_{DDQ}$ + 0.3 | V |
| $V_{IL\ (DC)}$ | Input Low (Logic0) Voltage | -0.3 | $V_{REF}$ – 0.125 | -0.3 | $V_{REF}$ – 0.125 | V |


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## Operating, Standby, and Refresh Currents

$T_{CASE}$ = 0 °C ~ 85 °C; $V_{DDQ}$ = $V_{DD}$ = 1.8V ± 0.1V [1GB, 2 Ranks, 64Mx16 DDR2 SDRAMs]

| Symbol | Parameter/Condition | PC2-5300 (-3C) | PC2-6400 (-AC) | Unit |
|---|---|---|---|---|
| IDD0 | Operating Current: one bank; active/precharge; $t_{RC}$ = $t_{RC\ (MIN)}$; $t_{CK}$ = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle | 660 | 792 | mA |
| IDD1 | Operating Current: one bank; active/read/precharge; Burst = 4; $t_{RC}$ = $t_{RC\ (MIN)}$; CL= 4; $t_{CK}$ = $t_{CK\ (MIN)}$; $I_{OUT}$ = 0mA; address and control inputs changing once per clock cycle | 748 | 858 | mA |
| IDD2P | Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; $t_{CK}$ = $t_{CK\ (MIN)}$ | 79 | 79 | mA |
| IDD2Q | Precharge quiet standby current | 440 | 528 | mA |
| IDD2N | Idle Standby Current: CS ≥ $V_{IH\ (MIN)}$; all banks idle; CKE ≥ $V_{IH\ (MIN)}$; $t_{CK}$ = $t_{CK\ (MIN)}$; address and control inputs changing once per clock cycle | 440 | 572 | mA |
| IDD3N | Active Standby Current: one bank; active/precharge; CS ≥ $V_{IH\ (MIN)}$; CKE ≥ $V_{IH\ (MIN)}$; $t_{RC}$ = $t_{RAS\ (MAX)}$; $t_{CK}$ = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle | 506 | 616 | mA |
| IDD4R | Operating Current: one bank; Burst = 4; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 4; $t_{CK}$ = $t_{CK\ (MIN)}$; $I_{OUT}$ = 0mA | 880 | 1320 | mA |
| IDD4W | Operating Current: one bank; Burst = 4; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL= 4; $t_{CK}$ = $t_{CK\ (MIN)}$ | 880 | 1320 | mA |
| IDD5B | Burst Refresh Current: $t_{RC}$ = $t_{RFC\ (MIN)}$ | 1100 | 1210 | mA |
| IDD6 | Self-Refresh Current: CKE ≤ 0.2V | 79 | 79 | mA |
| IDD7 | Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; $t_{RC}$ = $t_{RC\ (min)}$; $I_{OUT}$ = 0mA. | 1364 | 1738 | mA |
| Note: Module IDD was calculated from component IDD. It may differ from the actual measurement. | | | | |


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## Operating, Standby, and Refresh Currents

$T_{CASE}$ = 0 °C ~ 85 °C; $V_{DDQ}$ = $V_{DD}$ = 1.8V ± 0.1V [2GB, 2 Ranks, 128M x 8 DDR2 SDRAMs]

| Symbol | Parameter/Condition | PC2-5300 (-3C) | PC2-6400 (-AC) | Unit |
|---|---|---|---|---|
| IDD0 | Operating Current: one bank; active/precharge; $t_{RC}$ = $t_{RC\ (MIN)}$; $t_{CK}$ = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle | 836 | 968 | mA |
| IDD1 | Operating Current: one bank; active/read/precharge; Burst = 4; $t_{RC}$ = $t_{RC\ (MIN)}$; CL= 4; $t_{CK}$ = $t_{CK\ (MIN)}$; $I_{OUT}$ = 0mA; address and control inputs changing once per clock cycle | 924 | 1100 | mA |
| IDD2P | Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; $t_{CK}$ = $t_{CK\ (MIN)}$ | 158 | 158 | mA |
| IDD2Q | Precharge quiet standby current | 528 | 616 | mA |
| IDD2N | Idle Standby Current: CS ≥ $V_{IH\ (MIN)}$; all banks idle; CKE ≥ $V_{IH\ (MIN)}$; $t_{CK}$ = $t_{CK\ (MIN)}$; address and control inputs changing once per clock cycle | 528 | 704 | mA |
| IDD3N | Active Standby Current: one bank; active/precharge; CS ≥ $V_{IH\ (MIN)}$; CKE ≥ $V_{IH\ (MIN)}$; $t_{RC}$ = $t_{RAS\ (MAX)}$; $t_{CK}$ = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle | 660 | 792 | mA |
| IDD4R | Operating Current: one bank; Burst = 4; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 4; $t_{CK}$ = $t_{CK\ (MIN)}$; $I_{OUT}$ = 0mA | 1144 | 1408 | mA |
| IDD4W | Operating Current: one bank; Burst = 4; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL= 4; $t_{CK}$ = $t_{CK\ (MIN)}$ | 1144 | 1408 | mA |
| IDD5B | Burst Refresh Current: $t_{RC}$ = $t_{RFC\ (MIN)}$ | 1672 | 1892 | mA |
| IDD6 | Self-Refresh Current: CKE ≤ 0.2V | 158 | 158 | mA |
| IDD7 | Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; $t_{RC}$ = $t_{RC\ (min)}$; $I_{OUT}$ = 0mA. | 2112 | 2552 | mA |
| Note: Module IDD was calculated from component IDD. It may differ from the actual measurement. | | | | |


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## AC Timing Specifications for DDR2 SDRAM Devices Used on Module

($T_{CASE}$ = 0 °C ~ 85 °C; $V_{DDQ}$ = 1.8V ± 0.1V; $V_{DD}$ = 1.8V ± 0.1V, See AC Characteristics) (Part 1 of 2)

| Symbol | Parameter | -3C | | -AC | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{AC}$ | DQ output access time from CK/$\overline{CK}$ | -0.45 | +0.45 | -0.40 | +0.40 | ns | |
| $t_{DQSCK}$ | DQS output access time from CK/$\overline{CK}$ | -0.4 | +0.4 | -0.35 | +0.35 | ns | |
| $t_{CH}$ | CK high-level width | 0.48 | 0.52 | 0.48 | 0.52 | $t_{CK}$ | |
| $t_{CL}$ | CK low-level width | 0.48 | 0.52 | 0.48 | 0.52 | $t_{CK}$ | |
| $t_{HP}$ | Minimum half clk period for any given cycle; defined by clk high ($t_{CH}$) or clk low ($t_{CL}$) time | Min(tCH(abs),tCL(abs)) | - | Min(tCH(abs),tCL(abs)) | - | $t_{CK}$ | |
| $t_{CK}$ | Clock Cycle Time | 3 | 8 | 2.5 | 8 | ns | |
| $t_{DH}$ | DQ and DM input hold time | 175 | - | 125 | - | ps | |
| $t_{DS}$ | DQ and DM input setup time | 100 | - | 50 | - | ps | |
| $t_{IPW}$ | Input pulse width | 0.6 | - | 0.6 | - | $t_{CK}$ | |
| $t_{DIPW}$ | DQ and DM input pulse width (each input) | 0.35 | - | 0.35 | - | $t_{CK}$ | |
| $t_{HZ}$ | Data-out high-impedance time from CK/$\overline{CK}$ | - | $t_{AC\ max}$ | - | $t_{AC\ max}$ | ns | |
| $t_{LZ(DQ)}$ | Data-out low-impedance time from CK/$\overline{CK}$ | $2xt_{AC\ min}$ | $t_{AC\ max}$ | $2xt_{AC\ min}$ | $t_{AC\ max}$ | ns | |
| $t_{LZ(DQS)}$ | DQS low-impedance time from CK/$\overline{CK}$ | $t_{AC\ min}$ | $t_{AC\ max}$ | $t_{AC\ min}$ | $t_{AC\ max}$ | ns | |
| $t_{DQSQ}$ | DQS-DQ skew (DQS & associated DQ signals) | - | 0.24 | - | 0.20 | ns | |
| $t_{QHS}$ | Data hold Skew Factor | - | 0.34 | - | 0.30 | ns | |
| $t_{QH}$ | Data output hold time from DQS | $t_{HP} - t_{QHS}$ | - | $t_{HP} - t_{QHS}$ | - | ns | |
| $t_{DQSS}$ | Write command to 1st DQS latching transition | -0.25 | 0.25 | -0.25 | 0.25 | $t_{CK}$ | |
| $t_{DQSH}$ | DQS input high pulse width | 0.35 | - | 0.35 | - | $t_{CK}$ | |
| $t_{DQSL}$ | DQS input low pulse width | 0.35 | - | 0.35 | - | $t_{CK}$ | |
| $t_{DSS}$ | DQS falling edge to CK setup time (write cycle) | 0.2 | - | 0.2 | - | $t_{CK}$ | |
| $t_{DSH}$ | DQS falling edge hold time from CK (write cycle) | 0.2 | - | 0.2 | - | $t_{CK}$ | |
| $t_{MRD}$ | Mode register set command cycle time | 2 | - | 2 | - | $t_{CK}$ | |
| $t_{WPST}$ | Write postamble | 0.40 | 0.60 | 0.40 | 0.60 | $t_{CK}$ | |
| $t_{WPRE}$ | Write preamble | 0.35 | - | 0.35 | - | $t_{CK}$ | |
| $t_{IH}$ | Address and control input hold time | 0.275 | - | 0.250 | - | ns | |
| $t_{IS}$ | Address and control input setup time | 0.2 | - | 0.175 | - | ns | |
| $t_{RPRE}$ | Read preamble | 0.9 | 1.1 | 0.9 | 1.1 | $t_{CK}$ | |
| $t_{RPST}$ | Read postamble | 0.4 | 0.6 | 0.4 | 0.6 | $t_{CK}$ | |
| $t_{Delay}$ | Minimum time clocks remains ON after CKE asynchronously drops Low | $t_{IS} + t_{CK(avg)} + t_{IH}$ | - | $t_{IS} + t_{CK(avg)} + t_{IH}$ | - | ns | |
| $t_{RFC}$ | Refresh to active/Refresh command time | 127.5 | | 127.5 | | ns | |
| $t_{REFI}$ | Average Periodic Refresh Interval (85ºC < $T_{CASE}$ ≤ 95ºC) | 3.9 | | 3.9 | | µs | |
| | Average Periodic Refresh Interval (0ºC ≤ $T_{CASE}$ ≤ 85ºC) | 7.8 | | 7.8 | | µs | |


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## AC Timing Specifications for DDR2 SDRAM Devices Used on Module

($T_{CASE}$ = 0 °C ~ 85 °C; $V_{DDQ}$ = 1.8V ± 0.1V; $V_{DD}$ = 1.8V ± 0.1V, See AC Characteristics) (Part 2 of 2)

| Symbol | Parameter | -3C | | -AC | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{RRD}$ | Active bank A to Active bank B command | 7.5 | - | 7.5 | - | ns | |
| $t_{CCD}$ | $\overline{CAS}$ to $\overline{CAS}$ | 2 | - | 2 | - | $t_{CK}$ | |
| $t_{WR}$ | Write recovery time | 15 | - | 15 | - | ns | |
| WR | Write recovery time with Auto-Precharge | $t_{WR}/t_{CK}$ | | $t_{WR}/t_{CK}$ | | ns | |
| $t_{DAL}$ | Auto precharge write recovery + precharge time | WR +$t_{nRP}$ | - | WR +$t_{nRP}$ | - | $t_{CK}$ | |
| $t_{WTR}$ | Internal write to read command delay | 7.5 | - | 7.5 | - | ns | |
| $t_{RTP}$ | Internal read to precharge command delay | 7.5 | - | 7.5 | - | ns | |
| $t_{XSNR}$ | Exit self refresh to a Non-read command | $t_{RFC}$ +10 | - | $t_{RFC}$ +10 | - | ns | |
| $t_{XSRD}$ | Exit self refresh to a Read command | 200 | - | 200 | - | $t_{CK}$ | |
| $t_{XP}$ | Exit precharge power down to any Non- read command | 2 | - | 2 | - | $t_{CK}$ | |
| $t_{XARD}$ | Exit active power down to read command | 2 | - | 2 | - | $t_{CK}$ | |
| $t_{XARDS}$ | Exit active power down to read command | 7-AL | - | 8-AL | - | $t_{CK}$ | |
| $t_{CKE}$ | CKE minimum pulse width | 3 | - | 3 | - | $t_{CK}$ | |
| $t_{OIT}$ | OCD drive mode output delay | 0 | 12 | 0 | 12 | ns | |
| **ODT** | | | | | | | |
| $t_{AOND}$ | ODT turn-on delay | 2 | 2 | 2 | 2 | $t_{CK}$ | |
| $t_{AON}$ | ODT turn-on | $t_{AC(min)}$ | $t_{AC(max)}$ +0.7 | $t_{AC(min)}$ | $t_{AC(max)}$ +0.7 | ns | |
| $t_{AONPD}$ | ODT turn-on (Power down mode) | $t_{AC(min)}$ +2 | 2 $t_{CK(avg)}$ + $t_{AC(max)}$+1 | $t_{AC(min)}$ +2 | 2 $t_{CK(avg)}$ + $t_{AC(max)}$+1 | ns | |
| $t_{AOFD}$ | ODT turn-off delay | 2.5 | 2.5 | 2.5 | 2.5 | $t_{CK}$ | |
| $t_{AOF}$ | ODT turn-off | $t_{AC(min)}$ | $t_{AC(max)}$+0.6 | $t_{AC(min)}$ | $t_{AC(max)}$+0.6 | ns | |
| $t_{AOFPD}$ | ODT turn-off (Power down mode) | $t_{AC(min)}$ +2 | 2.5$t_{CK(avg)}$ + $t_{AC(max)}$+1 | $t_{AC(min)}$ +2 | 2.5$t_{CK(avg)}$ + $t_{AC(max)}$+1 | ns | |
| $t_{ANPD}$ | ODT to power down entry latency | 3 | - | 3 | - | $t_{CK}$ | |
| $t_{AXPD}$ | ODT power down exit latency | 8 | - | 8 | - | $t_{CK}$ | |

| Speed Grade Definition | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | -3C | | -AC | | Unit |
| | | Min. | Max. | Min. | Max. | |
| $t_{RAS}$ | Row Active Time | 45 | 70000 | 45 | 70000 | ns |
| $t_{RCD}$ | RAS to CAS delay | 15 | - | 12.5 | - | ns |
| $t_{RC}$ | Row Cycle Time | 60 | - | 57.5 | - | ns |
| $t_{RP}$ | Row Precharge Time | 15 | - | 12.5 | - | ns |


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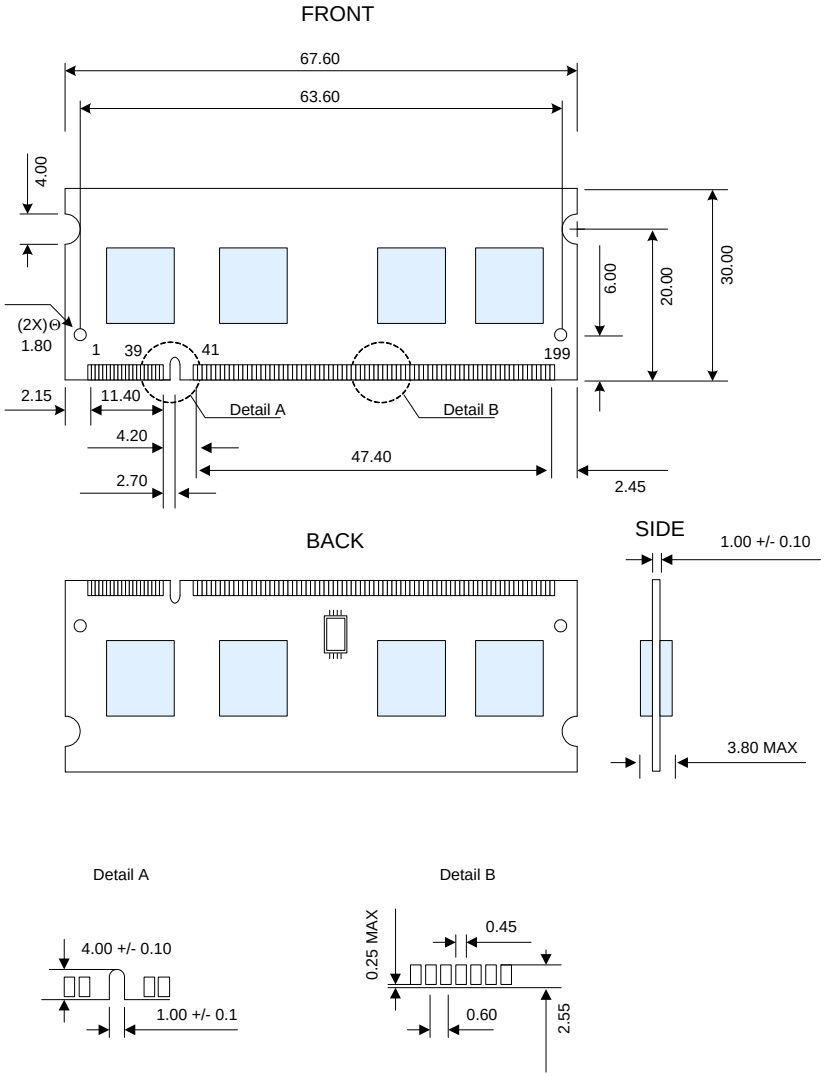
## Package Dimensions

[1GB – 2 Ranks, 64Mx16 DDR2 SDRAMs]




Note: All dimensions are typical with tolerances of +/- 0.15 unless otherwise stated.
Units: Millimeters (Inches)

Note: Device position and scale are only for reference.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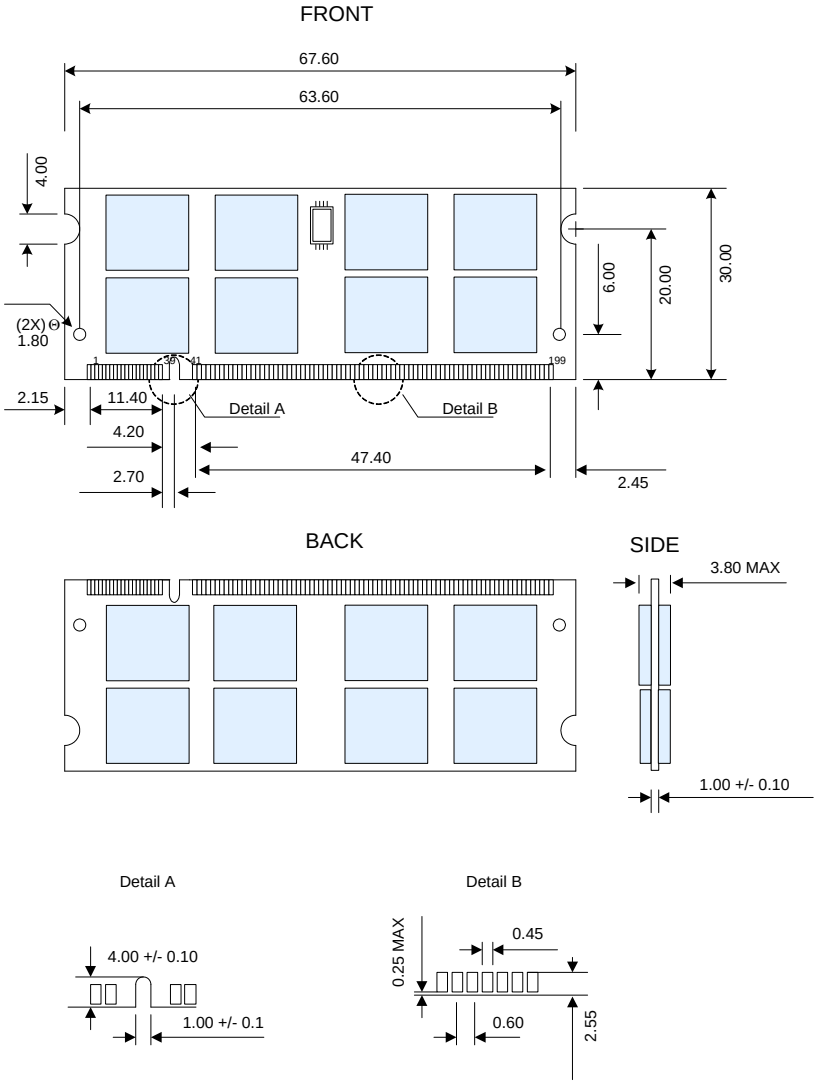
## Package Dimensions

[2GB – 2 Ranks, 128M x8 DDR2 SDRAMs]




Note: All dimensions are typical with tolerances of +/- 0.15 unless otherwise stated.
Units: Millimeters (Inches)

Note: Device position and scale are only for reference.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## Revision Log

| Rev | Date | Modification |
|---|---|---|
| 0.1 | 01/2010 | Preliminary Edition |
| 1.0 | 07/2010 | Official Release |

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